

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:	:	
	:	
Feng CHEN	:	Art Unit: ____
	:	
Application No. ____	:	Examiner: ____
	:	
Filed herewith: November 26, 2003	:	Atty Docket: TI-35189

For: SUPPRESSING DIGITAL-TO-ANALOG CONVERTER (DAC) ERROR

INFORMATION DISCLOSURE STATEMENT

and

NOTICE OF RELATED APPLICATION

Mail Stop Patent Application
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

The **Fattaruso *et al.*** article discloses use of analog self-calibration and dynamic element matching to enhance linearity of digital-to-analog converters (DACs) in the context of sigma-delta modulators (SDMs) for high-precision analog-to-digital conversion.

The **Chen *et al.*** article (whose lead author is the present inventor) discloses a second-order sigma delta modulator having a three-bit internal quantizer, in which an individual level averaging scheme is used to eliminate harmonic distortion due to element mismatch.

The **Baird *et al.*** article discloses a dynamic element matching (DEM) algorithm termed "data weighted averaging" (DWA), for use in multi-bit delta sigma data converters.

The **Fujimori *et al.*** article, mentioned in the Background of the Invention with reference to Applicant's FIG. 4, discloses a fourth-order cascaded delta sigma modulator that employs Multibit quantization and dynamic element matching (DEM) to reduce quantization noise.

Notice of Related Application. U.S. Application No. 10/417,616, filed April 1, 2003, "System and Method for Dynamic Element Matching," names the same inventor as the present case. It is suggested that the examiner monitor prosecution of that case for cases that may be considered relevant to the present case.

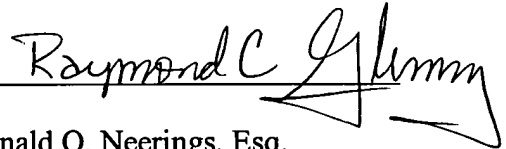
The examiner is respectfully requested to initial the space adjacent each document entry on the attached Form PTO-1449, and to return a copy of the initialled Form PTO-1449 to confirm that the accompanying documents have been considered and has been officially made of record in this application.

Respectfully submitted,

Date: November 26, 2003

Customer No. 23,494
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Atty Docket: TI-35189

By: _____


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Form PTO-1449 Information Disclosure Citation				Attorney Docket		Application No.		
				TI-35189				
				Applicant		Examiner		
				Feng CHEN				
				Application Filing Date		Group Art Unit		
				November 26, 2003				
U.S. Patent Documents								
Examiner Initials	Cite	Patent Number	Date	Name		Class	Sub-Class	Filing Date
	A							
	B							
	C							
	D							
	E							
Foreign Patent Documents								
Examiner Initials	Cite	Document Number	Date	Country	Name	Class	Sub-Class	Translation
	F							Yes No
	G							Yes No
	H							Yes No
Other Documents (Including Author, Title, Date, Pertinent Pages, etc.)								
	I	J. Fattaruso, S. Kiriaki, M. de Wit, and G. Warwar, "Self-Calibration Techniques for a Second-Order Multibit Sigma-Delta Modulator," <i>IEEE Journal of Solid-State Circuits</i> , Vol. 28, No. 12, pp. 1216-1223, December 1993.						
	J	F. Chen and B. Leung, "A High Resolution Multibit Sigma-Delta Modulator with Individual Level Averaging," <i>1994 Symposium on VLSI Circuits Digest of Technical Papers</i> , pp. 101-102, 1994.						
	K	R. Baird and T. Fiez, "Linearity Enhancement of Multibit Delta Sigma A/D and D/A Converters Using Data Weighted Averaging," <i>IEEE Transactions on Circuits and System—II: Analog and Digital Signal Processing</i> , Vol. 42, No. 12, pp. 753-762, December 1995.						
	L	I. Fujimori, L. Longo, A. Hairapetian, K. Seiyama, S. Kasic, J. Cao and S. Chan, "A 90 dB SNR, 2.5 MHz Output Rate ADC using Cascaded Multibit Delta Sigma Modulation at 8x Oversampling Ratio," <i>2000 IEEE International Solid-State Circuits Conference (ISSCC)</i> , (WA 20.3) (2000).						
Examiner Signature				Date Considered				
EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP § 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to Applicant.								